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| Faculty of Engineering and Technology | | | |
| Ramaiah University of Applied Sciences | | | |
| Department | Computer Science and Engineering | Programme | B. Tech. in CSE |
| Semester/Batch | 3rd Semester/2018 | | |
| Course Code | 19CSC204A | Course Title | Logic Design |
| Course Leaders | Mr. Narasimha Murthy K. R. and Mr. V. Deepak | | |

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| Sections | Marking Scheme | | Marks | | |
| Max Marks | First Examiner Marks | Moderator |
| Question 1 |  | | | | |
| **A** | **Introduction** | **01** |  |  |
| **B** | **Circuit Design** | **04** |  |  |
| **C** | **Simulation of Circuit** | **03** |  |  |
| **D** | **Circuit using NAND Gates** | **02** |  |  |
|  | **Question 1 Max Marks** | **10** |  |  |
| Question 2 |  | | | | |
| **A** | **Introduction** | **01** |  |  |
| **B** | **Circuit Design** | **03** |  |  |
| **C** | **Simulation of Circuit** | **02** |  |  |
| **D** | **Circuit using Ex-OR Gates** | **04** |  |  |
|  | **Question 2 Max Marks** | **10** |  |  |

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| Assignment | | | |
| Reg.No. | 18ETCS002121 | Name of Student | SUBHENDU MAJI |

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| **Course Marks Tabulation** | | | | |
| **Component-1 (C) Assignment** | **First Examiner** | **Remarks** | **Moderator** | **Remarks** |
| **Question 1** |  |  |  |  |
| **Question 2** |  |  |  |  |
| **Marks (out of 20 )** |  |  |  |  |
| **Signature of First Examiner Signature of Moderator** | | | | |

**Note to Students**

1. The last date for assignment submission is **11th November 2019.**
2. Restrict the document to a maximum of 10 pages
3. The printed assignment must be submitted to the course leader
4. Documental evidence for all the components/parts of the assessment such as the reports, photographs, laboratory exam / tool tests are required to be attached to the assignment report in a proper order.
5. It is essential that all the sources used in preparation of the assignment must be suitably referenced in the text.

**Question 1 (10 Marks)**

Design and simulate a combinational circuit that functions as a binary calculator.

The circuit has four inputs: Two 2-bit numbers and one 2-bit code to represent the operation to be performed. Choose the number of outputs as needed.

Prepare a document, providing the solution in detail, with particular emphasis on:

1. Introduction to the functionality of the circuit
2. Circuit design using Logisim
3. Simulation of the designed circuit
4. Changes in the circuit if you had to implement it using only NAND gates

**Question 2 (10 Marks)**

Design and simulate a combinational circuit that generates 2’s complement of a 4-bit input binary number.

Prepare a document, providing the solution in detail, with particular emphasis on:

1. Introduction to the functionality of the circuit
2. Circuit design in Logisim using only basic gates
3. Simulation of the designed circuit
4. Circuit construction with only Ex-OR gates

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